

## AOD404

### N-Channel Enhancement Mode Field Effect Transistor

#### General Description

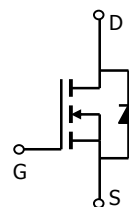
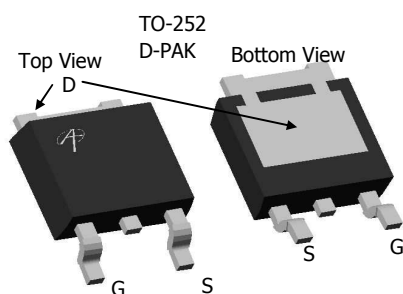
The AOD404 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and low gate resistance. This device is ideally suited for use as a high side switch in CPU core power conversion.

- RoHS Compliant
- Halogen Free\*

#### Features

- $V_{DS}$  (V) = 30V
- $I_D$  = 85A ( $V_{GS}$  = 10V)
- $R_{DS(ON)} < 7m\Omega$  ( $V_{GS}$  = 10V)
- $R_{DS(ON)} < 8m\Omega$  ( $V_{GS}$  = 4.5V)

**UIS TESTED!**  
**Rg, Ciss, Coss, Crss Tested**



#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>B,G</sup>	$I_D$	$T_C=25^\circ\text{C}^G$	85
		$T_C=100^\circ\text{C}^B$	65
Pulsed Drain Current	$I_{DM}$	200	A
Avalanche Current <sup>C</sup>	$I_{AR}$	30	A
Repetitive avalanche energy $L=0.1\text{mH}^C$	$E_{AR}$	120	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	100
		$T_C=100^\circ\text{C}$	50
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2.5
		$T_A=70^\circ\text{C}$	1.6
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	14.2	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	39	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>C</sup>	$R_{\theta JL}$	0.8	1.5	$^\circ\text{C/W}$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 12\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1	1.6	2	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	85			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=20\text{A}$ $T_J=125^\circ\text{C}$		5.4 8.4	7 10.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=20\text{A}$		6.6	8	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=20\text{A}$		90		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.74	1	V
$I_S$	Maximum Body-Diode Continuous Current				85	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$		2100	2520	pF
$C_{oss}$	Output Capacitance			536		pF
$C_{rss}$	Reverse Transfer Capacitance			165	231	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$	0.5	0.95	1.2	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(4.5\text{V})$	Total Gate Charge	$V_{GS}=4.5\text{V}$ , $V_{DS}=15\text{V}$ , $I_D=20\text{A}$		19.7	24	nC
$Q_{gs}$	Gate Source Charge			3.6		nC
$Q_{gd}$	Gate Drain Charge			7.9		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $R_L=0.75\Omega$ , $R_{GEN}=3\Omega$		5.9	10	ns
$t_r$	Turn-On Rise Time			11	17	ns
$t_{D(off)}$	Turn-Off Delay Time			36.2	55	ns
$t_f$	Turn-Off Fall Time			12	18	ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		35	42	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		33	50	nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on  $1\text{in}^2$  FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on steady-state  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any a given application depends on the user's specific board design, and the maximum temperature fo  $175^\circ\text{C}$  may be used if the PCB or heatsink allows it.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F: These tests are performed with the device mounted on  $1\text{in}^2$  FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by the package current capability.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev 8: Sep 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

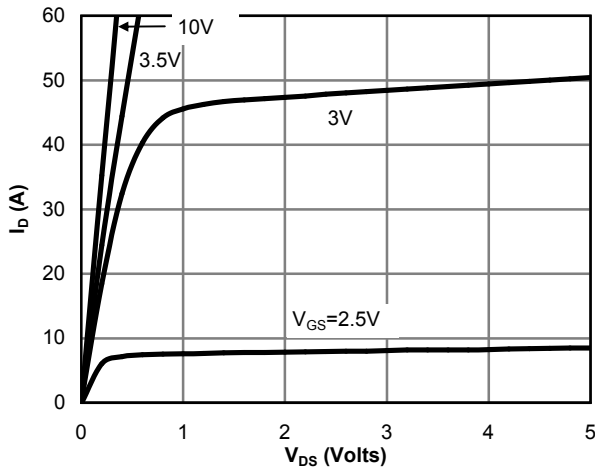


Fig 1: On-Region Characteristics

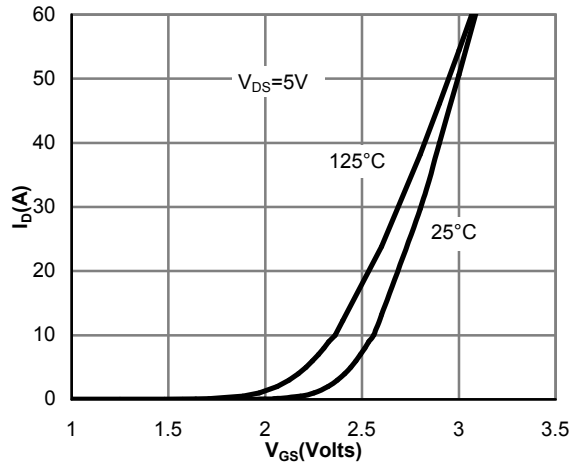


Figure 2: Transfer Characteristics

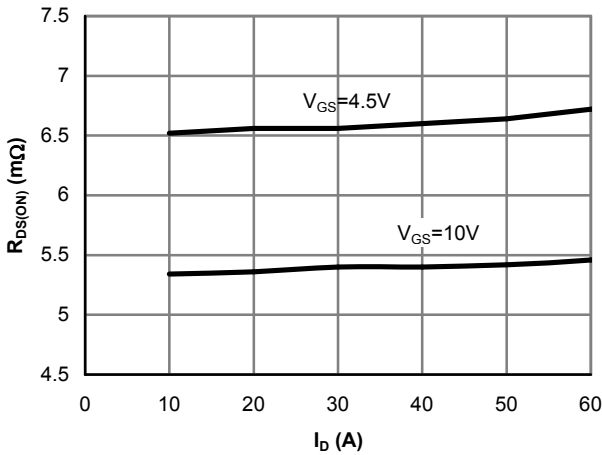


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

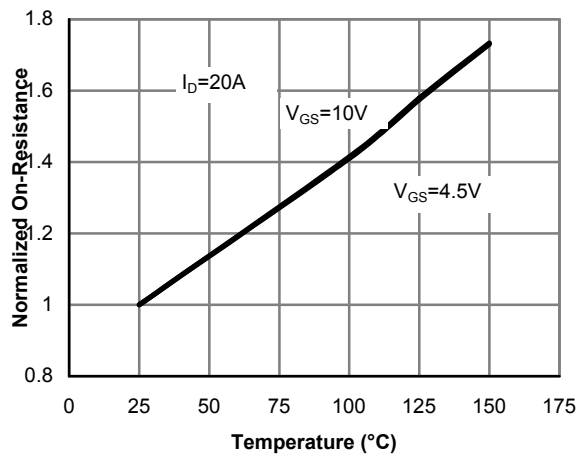


Figure 4: On-Resistance vs. Junction Temperature

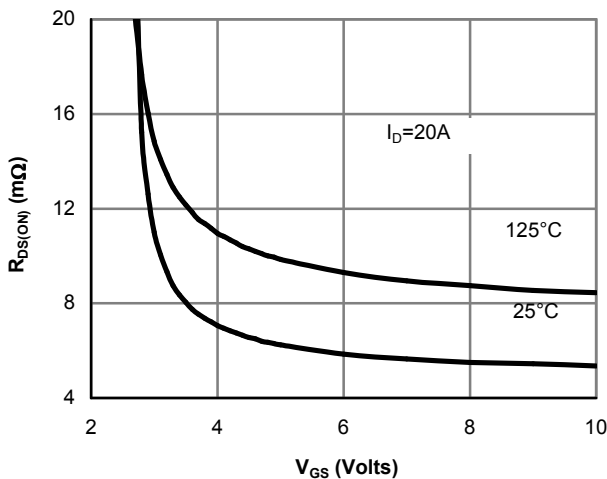


Figure 5: On-Resistance vs. Gate-Source Voltage

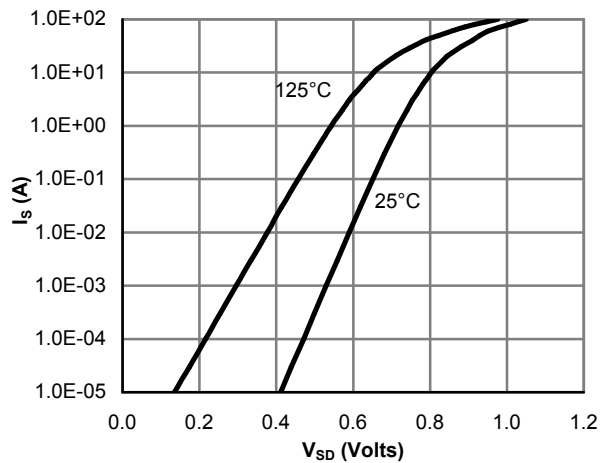


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

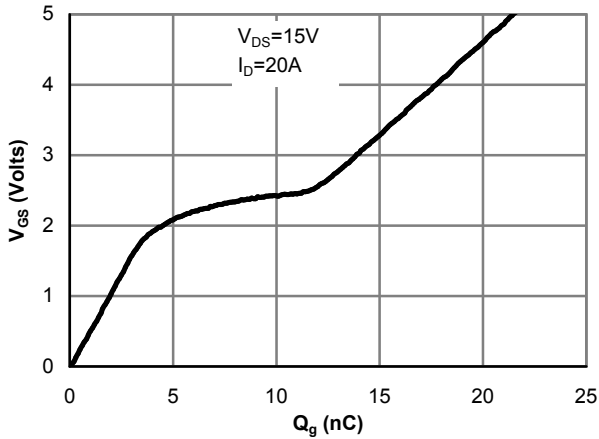


Figure 7: Gate-Charge Characteristics

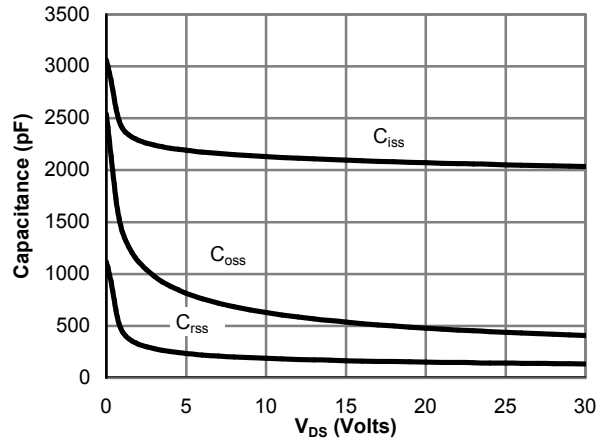


Figure 8: Capacitance Characteristics

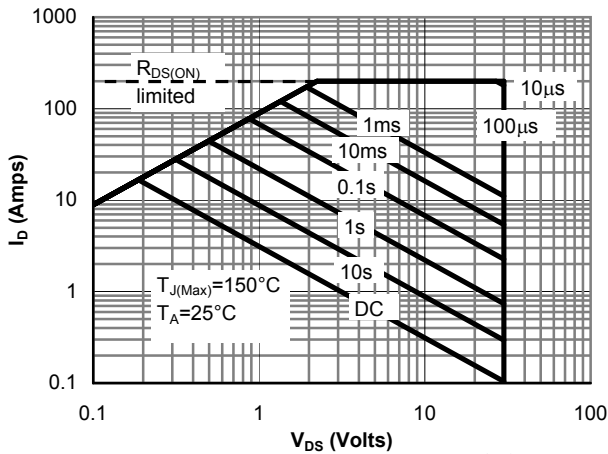


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

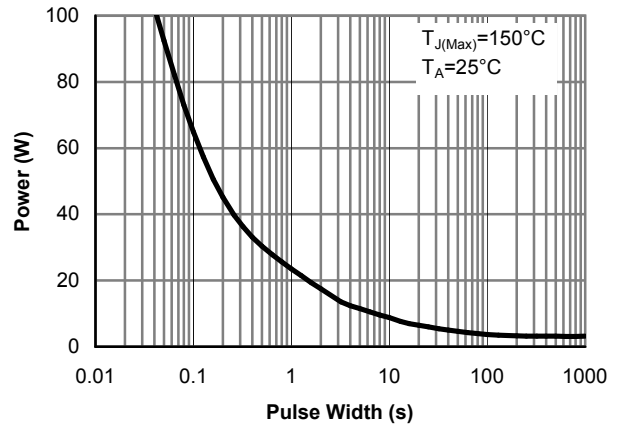


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

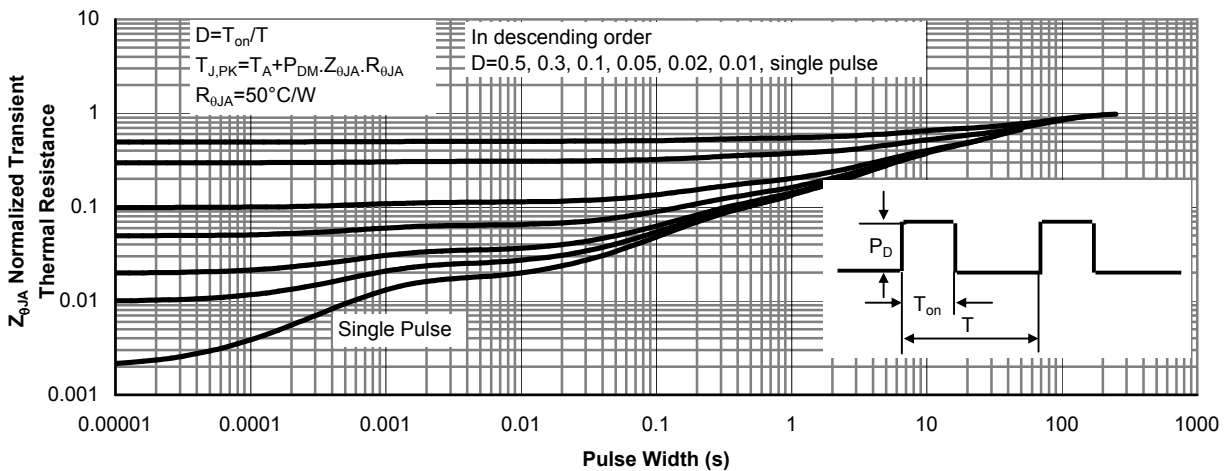


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

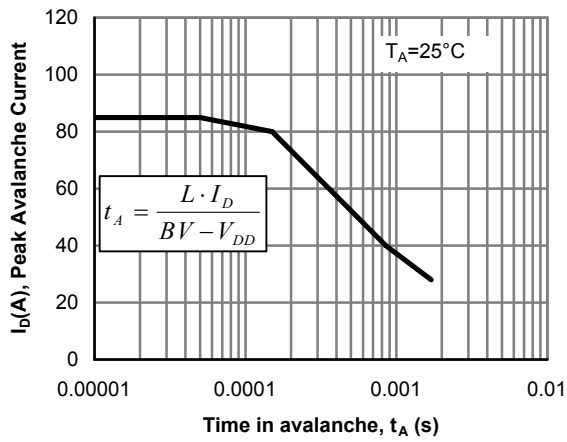


Figure 12: Single Pulse Avalanche capability

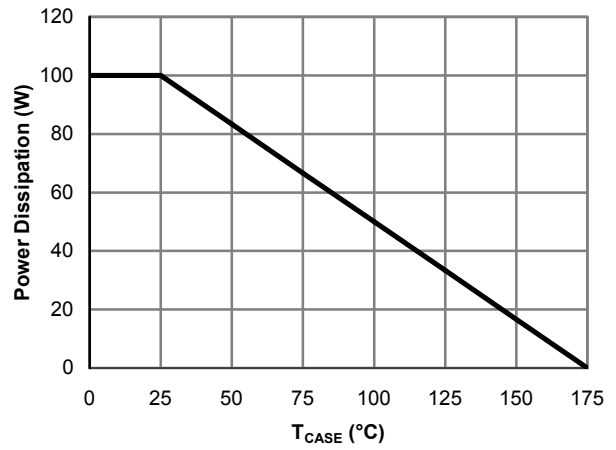


Figure 13: Power De-rating (Note B)

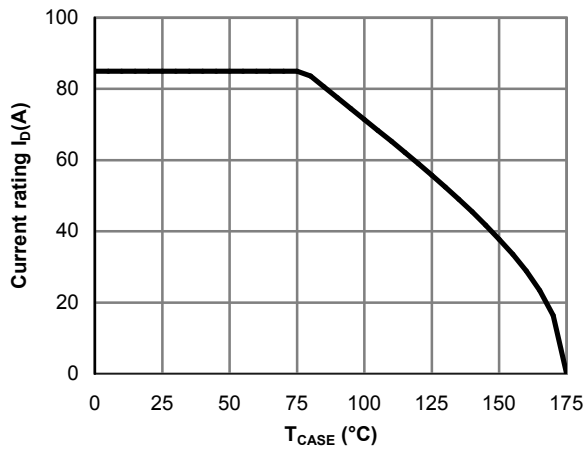
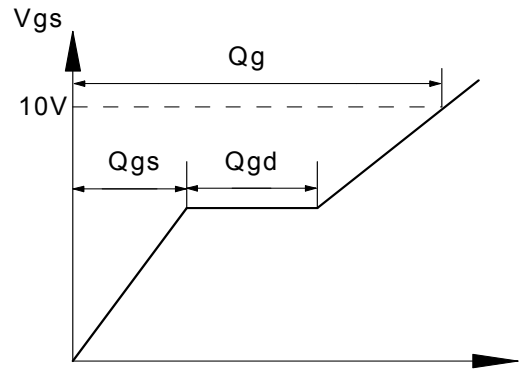
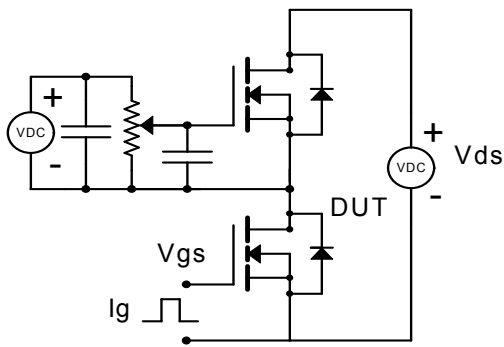
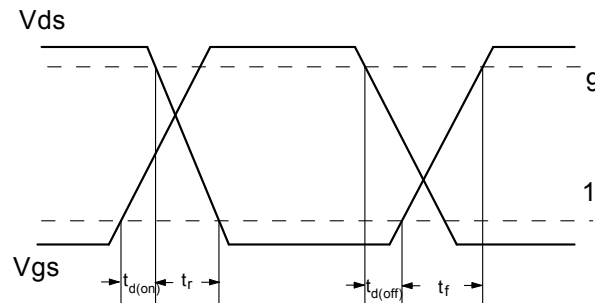
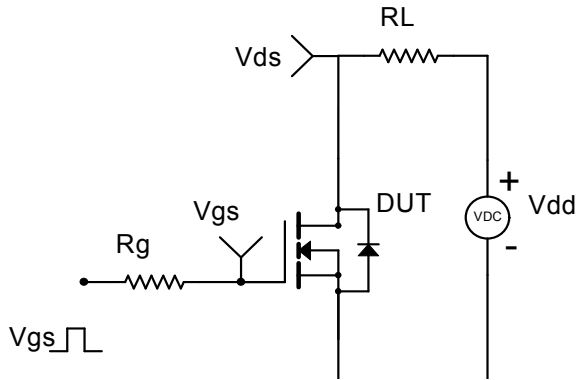


Figure 14: Current De-rating (Note B)

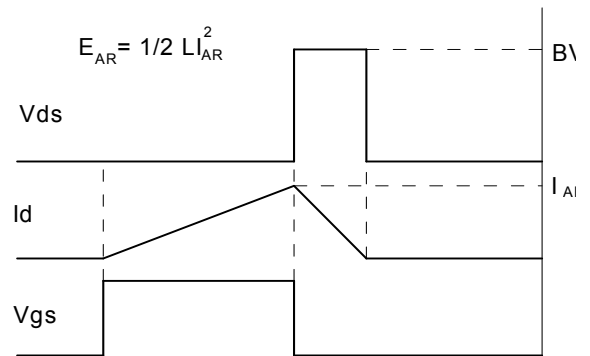
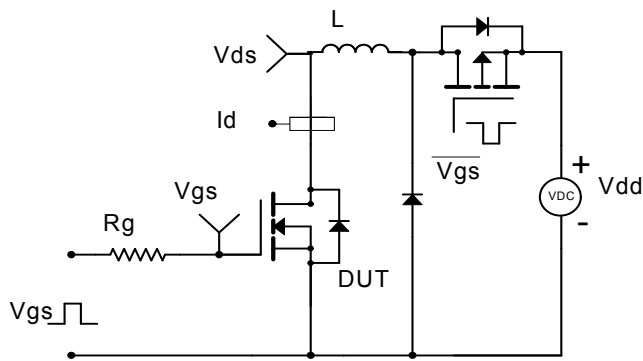
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

